

IBM Research & IBM Systems and Technology Group

C4NP

Technology for lead-free wafer bumping

September 2004

Outline

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- C4NP process description
 - Process flow
 - Bump template
 - C4NP bump plate characteristics
 - Bump template to wafer transfer
- C4NP advantages for lead-free solutions
- Lead-free opportunities for C4NP
- Conclusions

Announcement highlights

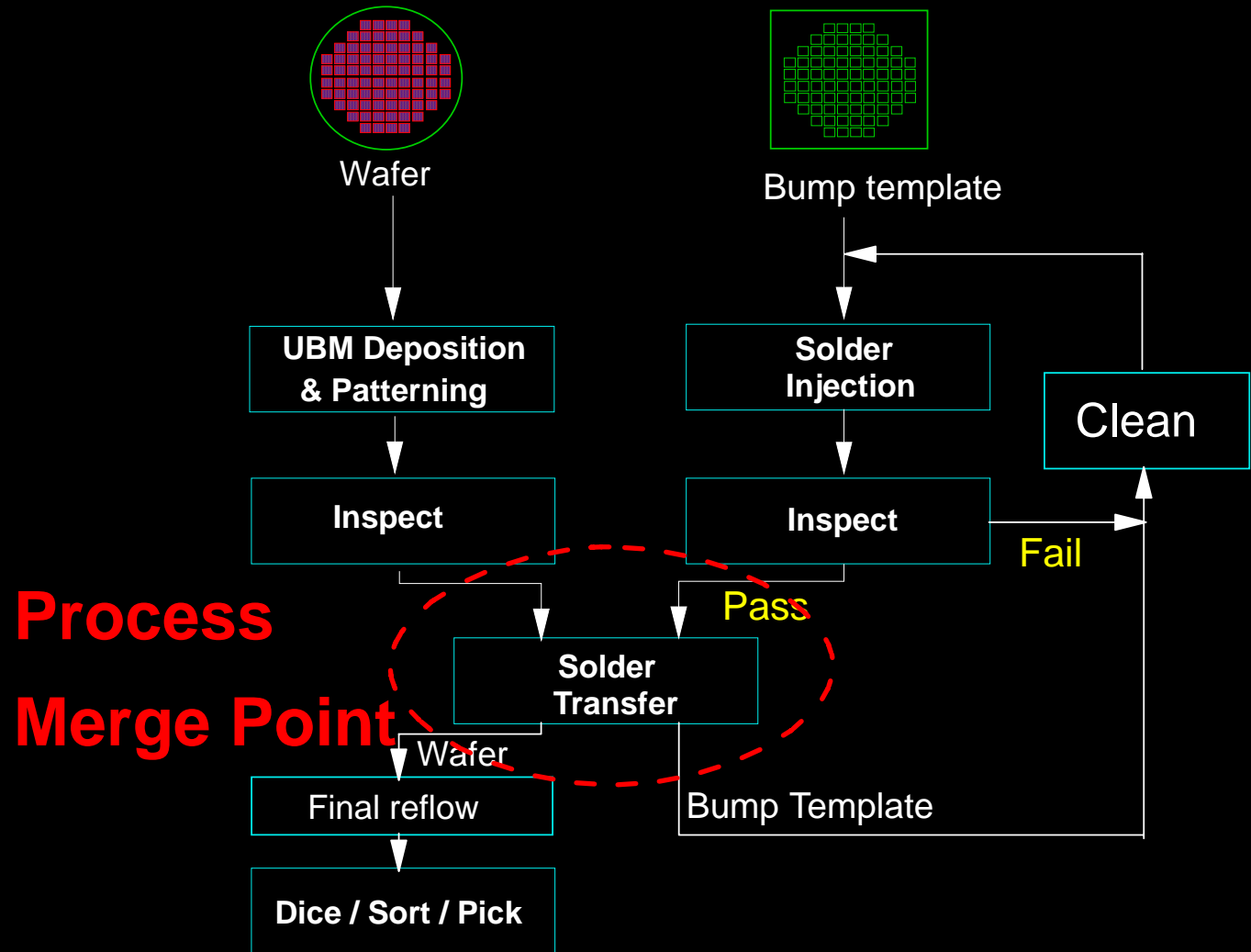
- This technology was pioneered at IBM's T.J. Watson Research Center and developed by IBM Microelectronics.
- IBM and SUSS MicroTec have signed an agreement to develop IBM's next-generation, 100 percent lead-free semiconductor packaging technology.
- This technology, C4NP (Controlled Collapse Chip Connection New Process), represents a breakthrough in semiconductor packaging.
- SUSS will develop a complete line of 300mm and 200mm equipment to enable commercialization of C4NP.
- C4NP could be a significant factor in allowing the industry to convert to a totally lead-free solution.
- IBM will continue advanced research and development of C4NP and offer on-site process training to customers who purchase commercial systems from SUSS.

C4NP Process Description

Bump template

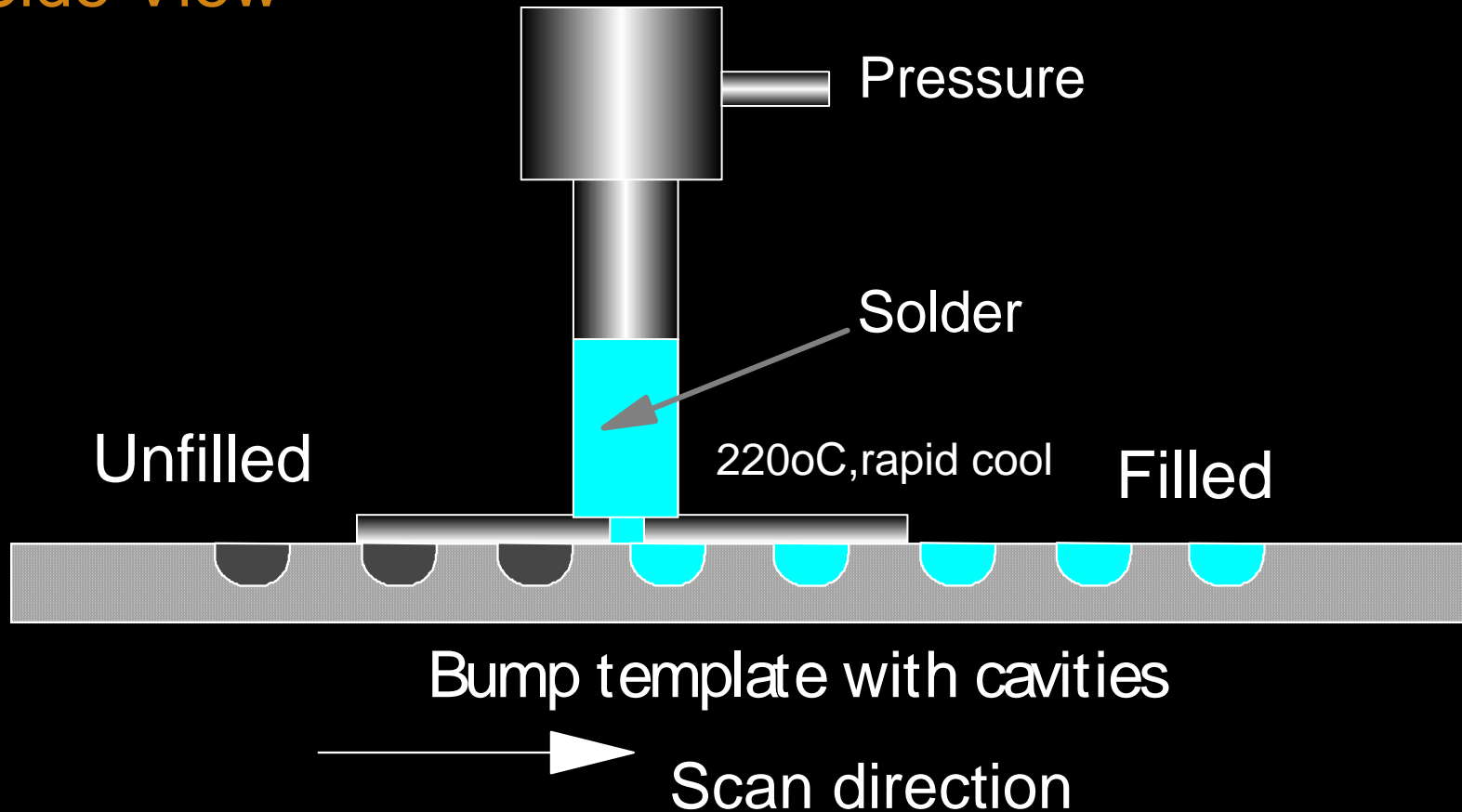
- Bulk solder in reservoir
- Head contacts bump template
- Reservoir heated above melting point
- Reservoir slightly pressurized
- Scan template to fill cavities
- Inspect (bump template is known to be good prior to transfer)
- Ready to commit to wafer transfer

C4NP Process Flow



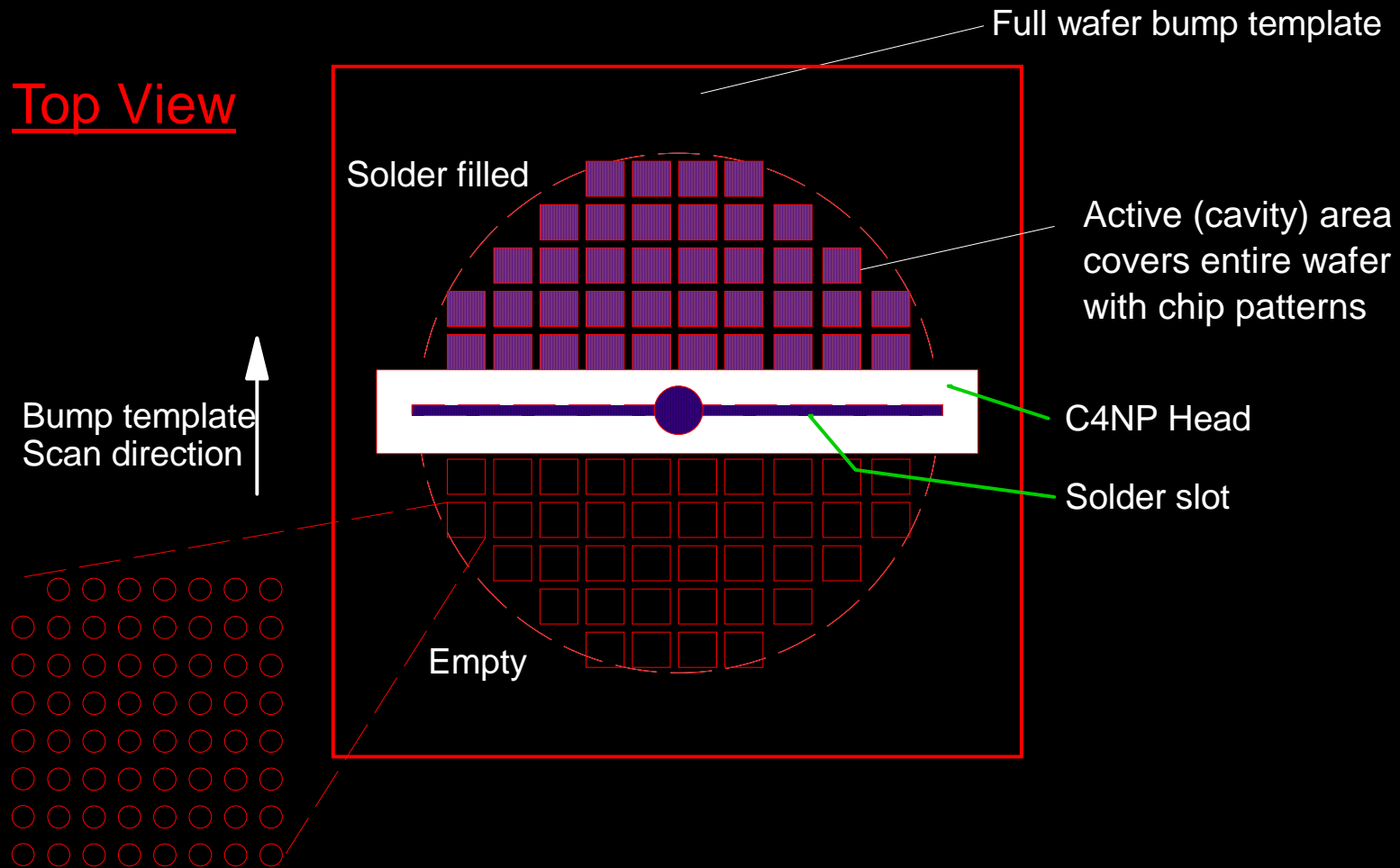
C4NP Process Description: Bump template fill

Side View



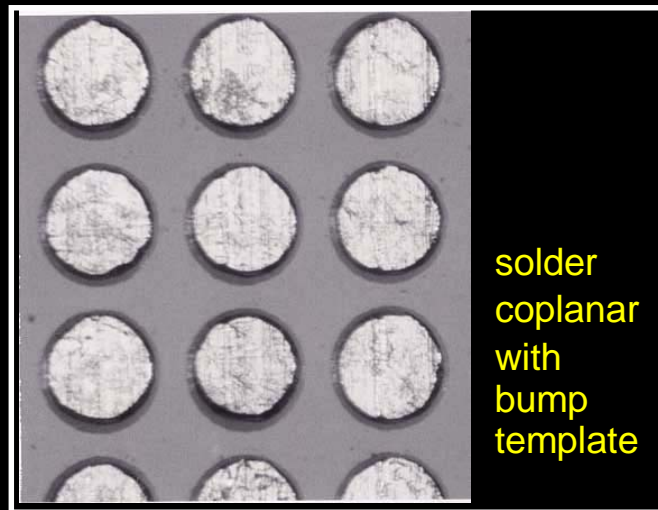
C4NP Process Description: Bump template fill

Top View



Each "chip pattern" is an array of cavities that matches pad array on chip

Typical C4NP Bump template



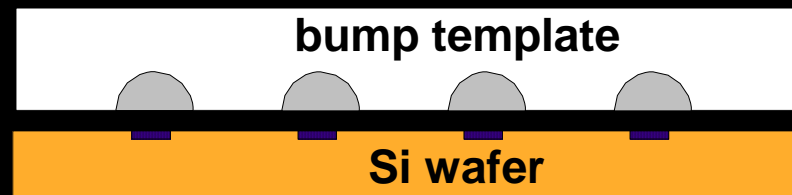
Diameter: 150um

Depth: 50um

Vol: $74 \times 10^{-3} \text{ um}^3$

C4NP Process Description

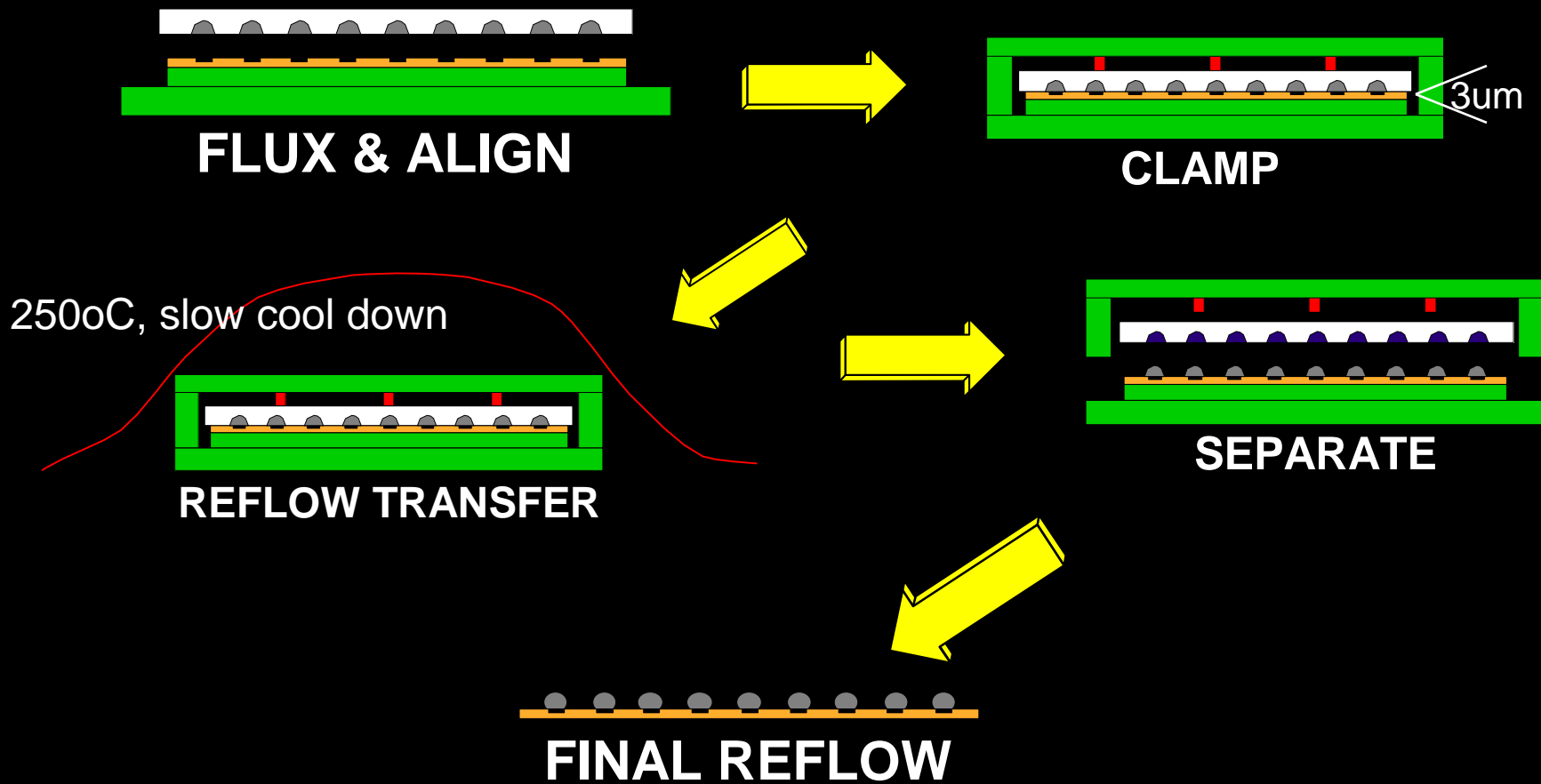
BUMP TEMPLATE CHARACTERISTICS



- **CTE matched to wafer**
- **Tightly controlled cavity volumes**
- **Common glass substrate used for template**
- **Template is reusable**

C4NP Process Description

WAFER-BUMP TRANSFER SEQUENCE



C4NP Process: Advantages

- Simplicity - process similar to stencil printing; bump templates scan under fixed solder head
- No volume change - finer bump size & pitch possible than with paste
- Known good template prior to transfer
- Low material cost - uses bulk alloy without converting to paste, pre-form, chemical solution
- Alloy independence – especially beneficial for ternary and quaternary lead-free alloys
- Efficient solder usage - environmental and economic benefits, especially with costlier alloys
- Rapid turn-around time – bump templates can be ready before wafers are finished

Lead-free opportunities for C4NP

- Help's address challenges of traditional bumping
- C4NP combines strengths of:
 - plating - extends to large 300mm wafers and fine bump size/pitch; minimal voids
 - paste screening - alloy independent including multi-component lead-free
- Eliminates weakness of:
 - evaporation - > 99% material wasted; limited to high-lead
- C4NP satisfies requirements given by ITRS:
 - process simplification
 - decreasing bump size/pitch
 - 300mm
 - lead-free
 - maintain quality, reliability and yield

Conclusions

- The convergence of flip chip growth, 300mm transition and lead-free requirements provide an opportunity for C4NP, a new bumping technology, developed by IBM, that combines high-end capabilities with low-end process simplicity
- With recent enhancements, C4NP has been extended to process lead-free alloys for wafer bumping
- Use of pure solder in a transfer process affords C4NP advantages in volume control, bump pitch, solder efficiency and alloy flexibility
- Improves cycle time